

REMARKS

1. Claim Rejections – 35 U.S.C. 102(e)

Claims 1 and 4 – 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Kataria.

5 Response

Claim 1

 Claim 1 contains the limitation “a counter for monitoring **the number of descriptors in a first state** to produce a count value”. As also detailed in Claim 1, the plurality of descriptors correspond to a subset of the plurality of data buffers to **manage** the received data packets. The first state corresponds to whether a buffer contains data or not. Kataria claims a system wherein **each** reassembly buffer has a **corresponding** counter, and the counter will decrement each time a new cell is stored in the buffer. As a buffer can store many cells, each decrement of the counter cannot correspond to a same state of the buffer. In addition, as the prior art cells are merely part of a data packet stored in the buffer (col. 1, lines 49-53 of Kataria’s disclosure), the applicant respectfully points out that Kataria’s cells enqueued in the buffer fail to read on applicant’s claimed descriptors utilized for managing received data packets. Therefore, the applicant asserts that Kataria fails to teach or suggest that the count value is obtained by monitoring **descriptors in a first state**. Furthermore, applicant’s threshold value and the count value concern the **plurality of buffers** as the plurality of descriptors correspond to a subset of the plurality of data buffers, whereas Kataria teaches a threshold value of one **single** buffer. Therefore, the first event being issued according to the comparison signal of Claim 1 will affect all of the plurality of buffers, not just a single buffer. In other words, the claimed limitation “a comparator for comparing the count value with the threshold value” is also not anticipated by Kataria.

 Briefly summarized, Kataria discloses a buffer management utilized for detecting

buffer overflow to terminate building of the current packet in the reassembly buffer by **comparison of each newly arrived cell with a threshold** (col. 2, lines 18-20 of Kataria's disclosure); however, applicant's apparatus of Claim 1 includes a counter for monitoring **the number of descriptors in a first state** to produce a count value and a comparator for
5 comparing the count value with the threshold, where **the descriptors correspond to data buffers and are defined to manage received data packets**.

In light of at least the above reasons, the applicant asserts that Kataria fails to teach or suggest all of the limitations recited in Claim 1. Therefore, Claim 1 should be found
10 patentable over the prior art. Reconsideration of Claim 1 is respectfully requested.

Claims 4 – 10

Claims 4 – 10 are dependent on Claim 1 and should therefore be found allowable if Claim 1 is found allowable.

Claim 11

15 Claim 11 describes the plurality of descriptors corresponding to a subset of the plurality of data buffers to manage the received data packets. Claim 11 further claims monitoring an amount of descriptors in a first state and comparing the amount with a threshold value. As detailed in the response to Claim 1, the counter taught by Kataria is decremented each time a cell is enqueued in a single buffer and therefore the
20 corresponding count value does not correspond to the state of **a plurality** of buffers (plurality of descriptors). In addition, Kataria's counted cells fail to read on applicant's claimed descriptors defined to manage received data packets. Furthermore, the threshold value taught by Kataria is a threshold value of **a single reassembly buffer** and not of a plurality of descriptors as in Claim 11.

25 For these reasons, and for the reasons detailed in the response to Claim 1, the applicant believes that Claim 11 should be found allowable over the prior art.

Reconsideration of Claim 11 is respectfully requested.

Claims 12 – 16

Claims 12 – 16 are dependent on Claim 11 and should therefore be found allowable if Claim 11 is found allowable.

5 Claim 17

Claim 17 has been amended to include the limitation that an amount of descriptors in a first state are monitored **when a plurality of error data packets are received**. As Kataria fails to disclose determining whether data packets contain errors, and further fails to disclose utilizing this determination result as a basis for adjusting the counter values
10 (counter values are adjusted according to the monitoring of descriptors in a first state), the applicant asserts that Kataria fails to teach or anticipate the added limitation. Therefore, the applicant asserts that currently amended Claim 17 should be found allowable over the prior art.

Claim 18

15 Claim 18 describes monitoring a number of descriptors corresponding to a number of data buffers that will have their state changed when a data packet is transferred and comparing that number to a threshold value. Kataria teaches monitoring a state of a single buffer, wherein transfer of each data packet to the buffer cannot be termed a different ‘state’ of that buffer. Furthermore, Claim 18 teaches changing the counter value each time
20 a state of a descriptor changes, i.e. there is only one count value for all the descriptors. As the count values taught by Kataria each correspond to a different respective buffer, there are many count values. Therefore, the count value taught in Claim 18 is different from the count value taught by Kataria.

For these reasons, and for the reasons detailed in the response to claims 1 and 11, the
25 applicant believes Claim 18 should be found allowable. Reconsideration of Claim 18 is

respectfully requested.

2. Claim Rejections – 35 U.S.C. 103(a)

Claims 2 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kataria in view of Tsujimoto.

5 Response

As claims 2 and 3 are dependent on Claim 1 and the applicant believes Claim 1 to have been placed in a position for allowance, claims 2 and 3 should also be found allowable.

10 3. New claims

Claim 19

Claim 19 has been added to include a masking circuit, for blocking an error signal when a data packet is an error data packet. As clearly stated in the applicant's disclosure, the purpose of the masking circuit is to prevent too many interrupts being generated to the system when data packets have errors. Kataria fails to teach or suggest a circuit for blocking error signals when error data packets are encountered, and further fails to provide motivation for adding a masking circuit, as Kataria does not teach methods related to encountering error data packets, and neither teaches nor anticipates adjusting counter values according to a positive determination of a data packet being an error data packet. Therefore, the applicant asserts that Kataria fails to teach the masking circuit of Claim 19, and new claim 19 should be found allowable. Furthermore, as Claim 19 is dependent on Claim 1 and the applicant believes Claim 1 to have been placed in a position for allowance, Claim 19 should also be found allowable.

Claim 20

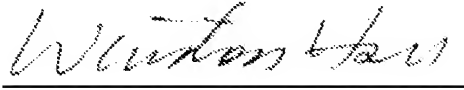
Claim 20 includes the limitation: “the counter monitors the number of the descriptors in the first state to produce the count value when the apparatus continuously receives a plurality of error data packets; wherein the counter is reset when the data packet is an ok data packet” wherein the counter value is adjusted when it is determined that the data packet is an error data packet. As clearly detailed in the specification, the purpose of this determination is to avoid too many interrupts to the system when the data packet has errors. As Kataria fails to disclose determining whether data packets contain errors, and further fails to disclose utilizing this determination result as a basis for adjusting the counter values, the applicant asserts that Kataria fails to teach or anticipate the added limitation. Furthermore, Kataria does not disclose resetting counter values when a data packet is an ok data packet. Therefore, the applicant asserts that new claim 20 should be found allowable. Furthermore, as Claim 20 is dependent on Claim 1 and the applicant believes Claim 1 to have been placed in a position for allowance, Claim 20 should also be found allowable.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Appl. No. 10/709,594
Amdt. dated October 18, 2007
Reply to Office action of July 18, 2007

Sincerely yours,



Date: 10.18.2007

Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)